NYMPH®

Crystal Clock Oscillator—Half Size HCMOS TRI-STATE

by SaRonix

T-50-23

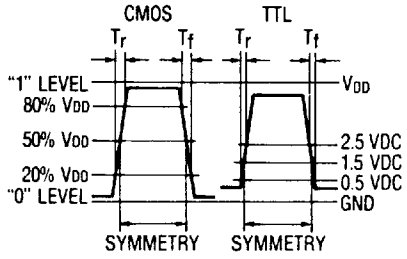
Technical Data

Ref. No. Series M
Date September 1990
Page 1 of 2

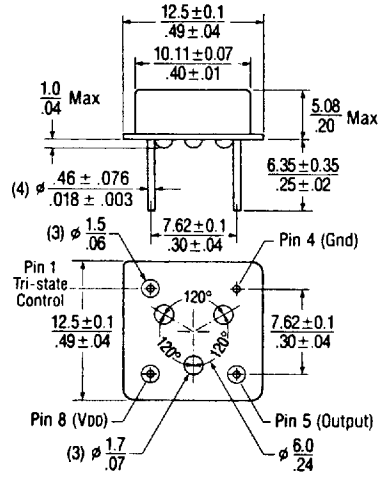
Description

A crystal controlled, low current hybrid oscillator providing precise rise and fall times to drive High Speed CMOS and NMOS microprocessors, like the Motorola 68000 family and INTEL 80386, 486 microprocessors. The third state in tri-state logic is an open circuit. The internal circuitry is disconnected from the output allowing it to assume any logic level. Can drive both High Speed CMOS and TTL. Device is packaged in a 1/2" × 1/2" resistance welded, all metal case to conserve board space.

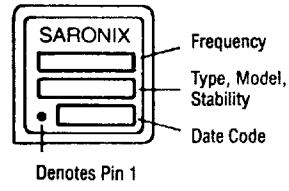
Output Waveform



Package



Standard Marking Format



Frequency Range:	500 kHz to 80 MHz
Frequency Stability:	±0.0025% to ±0.05% over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	
Operating:	0°C to +70°C
Storage:	–55°C to +125°C
Input Voltage:	
Recommended Operating:	+5 VDC ± 10%
Absolute Maximum:	+7 VDC
Input Current:	
500 kHz to 24 MHz:	15 mA max @ 25°C, 10 mA typical 20 mA max over operating temperature range
24+ MHz to 60 MHz:	30 mA max @ 25°C, 20 mA typical 35 mA max over operating temperature range
Above 60 MHz:	35 mA max @ 25°C, 30 mA typical 40 mA max over operating temperature range
Output Drive:	
CMOS	
Symmetry:	50% ± 5% @ .5 V_{DD}
Rise & Fall Times:	20% to 80% V_{DD}: T_r = 4 ns max, T_f = 4 ns max
Logic 0:	10% V_{DD} max
Logic 1:	90% V_{DD} min
Output Load:	150 pF max
TTL	
Symmetry:	50% ± 5% @ 1.5V level
Rise & Fall Times:	0.5 to 2.5V: T_r = 6 ns max, T_f = 4 ns max
Logic 0:	0.5V max
Logic 1:	2.5V min
Output Load:	150 pF max
Mechanical:	
Shock:	MIL-STD-883C, Method 2002, Condition B
Solderability:	MIL-STD-883C, Method 2003
Terminal Strength:	MIL-STD-202F, Method 211, Conditions A and C
Vibration:	MIL-STD-883C, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202F, Method 215
Resistance to Soldering Heat:	MIL-STD-202F, Method 210, Condition B
Environmental:	
Gross Leak Test:	MIL-STD-883C, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883C, Method 1014, Condition A2, <5 × 10^{-8} ATM cc/sec
Thermal Shock:	MIL-STD-883C, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883C, Method 1004

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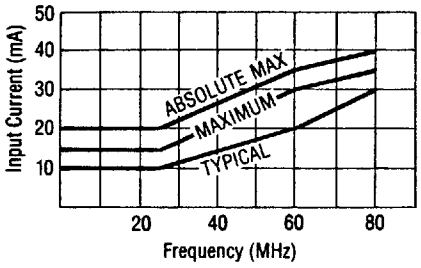
Current vs. Frequency



$R_L = 450\Omega$
$C_L = 30$ pF

Part Numbering Guide

NTH 0 39 C -4.0000

Type

Symmetry
0 = ±5% Symmetry
G = ±2.5% Symmetry

Model
39 = 500 kHz - 5.999 MHz
69 = 6.0000 MHz - 24.0000 MHz
89 = Above 24.0000 MHz

Stability Tolerance
A = ±25 ppm (0.0025%)
B = ±50 ppm (0.005%)
C = ±100 ppm (0.010%)
D = ±500 ppm (0.050%)

Frequency

Example PN: NTH089C – 32.0000 MHz

Test Circuits

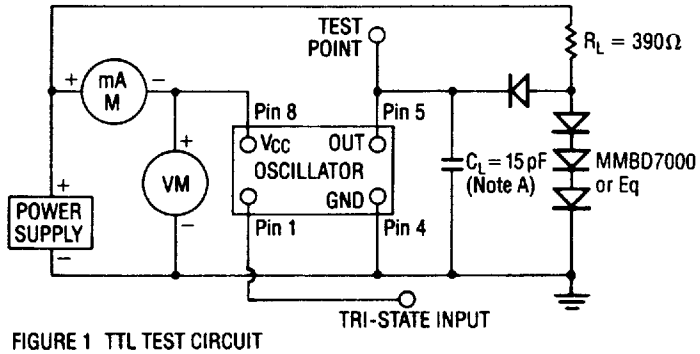


FIGURE 1 TTL TEST CIRCUIT

NOTE: A. C_L includes probe and jig capacitance.

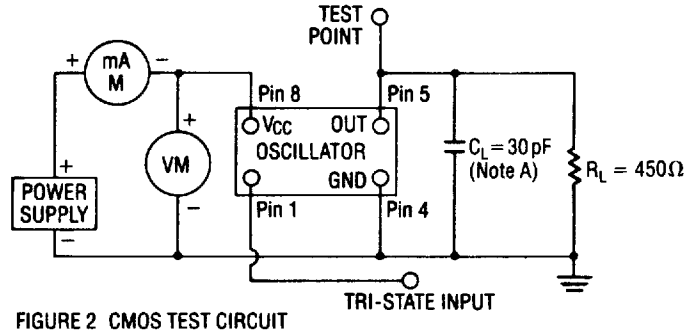


FIGURE 2 CMOS TEST CIRCUIT

NOTE: A. C_L includes probe and jig capacitance.

Tri-State Control:

Pin #1 = Control pin (Active high) with internal pull-up, 80 KΩ typical
Logic "1" or N.C. = Oscillator Signal Out
Logic "0" or GND = High Impedence on Pin #5 (typical output capacitance = 3 pF)

Required Input Levels on Pin 1:

Logic "1" = 3.0V min
Logic "0" = 0.5V max